REMARKS

By the present amendment claims 1, 4 and 13 have been amended to clarify the invention.

Claims 1-20 remain pending in the application.

In the Office Action, the Examiner objected to the drawings as failing to comply with 37 CFR §1.84(p)(5).

The Examiner objected to the title of the invention as being non-descriptive. Applicants respectfully submit that the title has been change to overcome the objection.

Claims 1, 4 and 13 were objected because of informalities. Applicants respectfully submit that claims 1, 4 and 13 have been amended to overcome the objection.

Claims 1-12 were rejected under 35 U.S.C. §112 as being indefinite.

Claims 1, 6-9, 12-13, 17 and 20 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Number 5,640,525 to Yumoto et al.

Claims 2-5 and 14-16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yumoto et al. in view of U.S. Patent Number 6,530,011 to Choquette.

Claims 10 and 18 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In view of the arguments that follow, Applicant respectfully traverses the Examiner's rejection of claims 1-9, 11-27 and 19-20.

Drawing Objections

The Examiner objected to the drawings as failing to comply with 37 C.F.R. §1.84(p)(5) because reference numbers 96A, 96B, and 83-88 in the specification is not mentioned in the drawings; the specification on page 14, lines 3-4 recites "0^{th} data 82" of Fig. 15, and in Fig. 15, reference number 82 is 6^{th} data; in Fig. 1, reference number 4 is labeled "IA" and the line between reference numbers 2 and 3 is labeled "IA."

Applicants respectfully submit that the specification has been amended to overcome the objection to Figure 15 of the drawings. Applicants also respectfully submit that Fig. 1 and Figure 13 have been amended to overcome the drawing objections. Therefore the objections should be withdrawn.

Rejection Under 35 U.S.C. §102(b)

The Examiner rejected claims 1, 6-9, 12-13, 17 and 20 under 35 U.S.C. §102(b) as being anticipated by Yumoto et al. The rejection is respectfully traversed.

The Examiner alleged that Yumoto et al. discloses the claimed invention of claim 1. Specifically, the Examiner alleged that Yumoto et al. discloses a waiting operation determination unit that determines an address by hash calculation from contents of the input packet (referencing col. 7, lines 11-12 and referring to a data pair generation mechanism: interleave flag, address generation circuit, and data select circuit which is defined by the Examiner as an address generation circuit that inherently generates or determines an address; referencing col. 4, lines 5-9 which is defined by the Examiner as showing that data from memory and the packet are check for hash collision which means

that the addresses must be generated by a hash calculation), selects one of a plurality of predetermined ways of processing waiting data (referencing col. 7, lines 12-15 which is defined by the Examiner as showing that one of a plurality of mechanisms for generating data is selected), outputs a select signal depending upon a combination of a data valid flag for said determined address, a constant valid flag read out by said constant readout unit, and the number of instruction inputs output from said instruction decoder for said waiting storage region (referencing col. 4, lines 24-35 which is defined by the Examiner as showing that a packet is output based on the number of inputs and a valid flag for data from the matching memory; referencing col. 11, lines 44-47 which is defined by the Examiner as showing that the selection is based off of a VLD flag; referencing col. 10, lines 20-22 which is defined by the Examiner as being the valid flag of the constant), and updates the data valid flag for said address based on the selected result (referencing col. 4, lines 31-35 which is defined by the Examiner as showing that the valid data flag (PRE) is updated).

Applicants respectfully submit that Yumoto et al. does not disclose or teach all the claimed limitations of the present invention. Among other things, the reference does not disclose "a waiting operation determination unit that determines a hash address by a hash calculation from contents of the input packet, selects one predetermined way out of a plurality of predetermined ways of processing waiting data, outputs a select signal for the predetermined way of processing waiting data depending upon a combination of a data valid flag for said determined hash address, a constant valid flag read out by said constant readout unit, and the number of instruction inputs output from said instruction decoder for

said waiting data storage region, and updates the data valid flag for said hash address based on the select predetermined way of processing waiting data," as recited in claim 1.

Yumoto et al. disclose a data pair generation mechanism that includes an interleave flag and an address generation circuit, and a data select circuit. The interleave flag and address generation circuit generates select information indicating which one of a plurality of dynamic data pair generation mechanism is to be selected and destination information included in an applied data packet. Yumoto et al. further discloses a hash collision detection unit that compares a hash overflow destination specifying portion in a matching memory with an hash overflow destination specifying portion in the input packet to determine whether a hash collision has occurred or not. When the input packet is determined as a 2-input instruction execution packet, and data read out from the matching memory is valid, and hash collision has occurred, a packet is output with a valid value of the hash collision flag. When the data read out from the matching memory is invalid, the data value in the input packet is written into an appropriate address of matching memory.

Applicants' disclose a "waiting operation determination unit" that calculates a hash address "from contents of the input packet" and selecting "one of a plurality of predetermined ways for processing waiting data," outputting "a select signal depending upon a combination of a data valid flag for said determined hash address, a constant valid flag read out by said constant readout unit, and the number of instruction inputs output from said instruction decoder for said waiting data storage region, and updates the data valid flag for said hash address based on the select predetermined way of processing waiting data." The hash collision detection unit that compares the hash overflow destination

specifying portion in the matching memory and the input packet of Yumoto et al. is not analogous to "a hash calculation from contents of the input packet" for determining a hash address. Moreover, select information indicating which of a plurality of dynamic data pair generation mechanism to be selected and destination information included in an applied data packet is not analogous to a waiting operation determination unit that "selects one predetermined way out of a plurality of predetermined ways for processing waiting data." Furthermore, the writing of the input packet into an appropriate address of matching memory and outputting the packet with a valid value of a hash collision flag of Yumoto et al. is not analogous to outputting "a select signal for the predetermined way of processing waiting data depending upon a combination of a data valid flag for said determined hash address, a constant valid flag read out by said constant readout unit, and the number of instruction inputs output from said instruction decoder for said waiting data storage region, and updates the data valid flag for said hash address based on the select predetermined way of processing waiting data."

Applicants respectfully submit that Yumoto et al. do not disclose or teach the claimed invention of claim and the rejection of claim 1 should be withdrawn.

Applicants respectfully submit that claim 13, which discloses "a waiting operation determination unit that determines a hash address by a hash calculation from contents of a the input packet, selects one predetermined way out of a plurality of predetermined ways of processing waiting data, outputs a select signal for the predetermined way of processing waiting data corresponding to a combination of a data valid flag for said determined address, a constant valid flag read out by said constant readout unit, and the number of instruction

inputs output from said instruction decoder for said waiting storage region, and updating the data valid flag for said hash address based on the selected predetermined way of processing waiting data," is analogous to claim 1 and is distinguishable over the prior art for at least the same reasons given above with regards to claim 1.

Dependent claims 2-9 and 12, which depend from claim 1, and claims 14-17 and 20, which depend from claim 13, are allowable for at least the same reasons with regards to claims 1 and 13 based on their dependency.

Conclusion

All objections and rejections raised in the Office Action having been addressed, it is respectfully submitted that the present application is in condition for allowance and such allowance is respectfully solicited. Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Demetra R. Smith-Stewart (Reg. No. 47,354), to conduct an interview in an effort to expedite prosecution in connection with the present application.

Pursuant to the provisions of 37 C.F.R. § 1.17 and §1.136(a), Applicant hereby petitions for an extension of one (1) month in which to file a response to the outstanding Office Action. The required fee of $110.00 is attached hereto.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1. 17; particularly, extension of time fees.

Respectfully submitted,

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